CLAIMS

What is claim is:

1. A simultaneous lamination process for forming a multiplayer substrate, at least comprising:
   (a) forming a plurality of laminating layers individually, wherein each said laminating layer has a dielectric layer with a first side and a second side, a patterned conductive layer positioned at the first side, and a plurality of first vias with a first ends and second ends positioned within the dielectric layer, wherein the first ends of the first vias connect with the patterned conductive layer and the second ends of the first vias are exposed by the dielectric layer at the second side;
   (b) forming a bottom layer having a second dielectric layer and a plurality of second vias penetrating the second dielectric layer; and
   (c) laminating said plurality of laminating layers and said bottom layer simultaneously to form the multiplayer substrate, wherein said bottom layer is disposed at a bottom side of the multiplayer substrate.

2. The lamination process according to claim1, further comprising a step of forming a metal layer on said second ends of the first vias.

3. The lamination process according to claim 2, wherein said metal layer is selected from one of solder, nickel gold alloy and a combination of solder and nickel gold alloy.

4. The lamination process according to claim 1, further comprising a step of forming two pad opening layers.

5. The lamination process according to claim 4, wherein said pad opening layer is a solder mask.

6. The lamination process according to claim 4, wherein said step (c) further comprising laminating said two pad opening layers simultaneously with said plurality of laminating layers and said bottom layer, wherein said two pad opening layers are disposed respectively at top and bottom sides of the multiplayer substrate.

7. A simultaneous lamination process for forming a multiplayer substrate, at least comprising:

(a) forming a plurality of laminating layers individually, wherein each said laminating layer has a dielectric layer with a first side and a second side, a patterned conductive layer positioned at the first side, and a plurality of first vias with a first ends and second ends positioned within the dielectric layer, wherein the first ends of the first vias connect with the patterned conductive layer and the second ends of the first vias are exposed by the dielectric layer at the second side;

(b) providing a core substrate with a plurality of through holes therein; and

(c) laminating said plurality of laminating layers and said core substrate simultaneously to form the multiplayer substrate.

8. The lamination process according to claim 7, further comprising a step of forming a metal layer on said second ends of the first vias.

9. The lamination process according to claim 7, wherein said metal layer is selected from one of solder, nickel gold alloy and a combination of solder and nickel gold alloy.

10. The lamination process according to claim 7, further comprising a step of forming two pad opening layers.

11. The lamination process according to claim 10, wherein said pad opening layer is a solder mask.

12. The lamination process according to claim 10, wherein said step (c) further comprising laminating said two pad opening layers simultaneously with said plurality of laminating layers and said core substrate, wherein said two pad opening layers are disposed respectively at top and bottom sides of the multiplayer substrate.

13. The lamination process according to claim 10, wherein said core substrate is disposed in the middle of the multiplayer substrate.

14. A lamination multiplayer substrate, at least comprising:

a plurality of laminating layers stacked and laminated together, wherein each said laminating layer has a dielectric layer with a first side and a second side, a patterned conductive layer positioned at the first side, and a plurality of first vias with a first ends and second ends positioned within the dielectric layer,

wherein the first ends of the first vias electrically connect with the patterned conductive layer and the second ends of the first vias electrically connect with an adjacent said laminating layer; and

a bottom layer stacked and laminated with the plurality of laminating layers and disposed at a bottom side of the multiplayer substrate, wherein said bottom layer has a second dielectric layer and a plurality of second vias penetrating the second dielectric layer and electrically connecting with the plurality of laminating layers, wherein said first dielectric layers and said second dielectric layer are bonded together.

15. The multiplayer substrate according to claim 14, further comprising two pad opening layers disposed respectively at top and bottom sides of the multiplayer substrate.

16. The multiplayer substrate according to claim 15, wherein said pad opening layer is a solder mask.

17. The multiplayer substrate according to claim 14, further comprising a metal layer disposed on said second ends of the vias.

18. The multiplayer substrate according to claim 17, wherein said metal layer is selected from one of solder, nickel gold alloy and a combination of solder and nickel gold alloy.

19. The multiplayer substrate according to claim 14, further comprising a heat sink disposed a top side of said multiplayer

substrate.

20.The multiplayer substrate according to claim 14, wherein said first and said second dielectric layers are selected from one of a thermal plastic resin and a thermal setting resin.

21. A lamination multiplayer substrate, at least comprising:
a core substrate having a plurality of through holes therein; and
a plurality of laminating layers stacked and laminated with said core substrate, wherein each said laminating layer has a dielectric layer with a first side and a second side, a patterned conductive layer positioned at the first side, and a plurality of vias with a first ends and second ends positioned within the dielectric layer, wherein the first ends of the vias electrically connect with the patterned conductive layer and the second ends of the first vias electrically connect with one of an adjacent said laminating layer and said core substrate, wherein said first dielectric layers are bonded together.

22. The multiplayer substrate according to claim 21, further comprising two pad opening layers disposed respectively at top and bottom sides of the multiplayer substrate.

23. The multiplayer substrate according to claim 22, wherein said pad opening layer is a solder mask.

24. The multiplayer substrate according to claim 21, further comprising a metal layer disposed on said second ends of the vias.

25. The multiplayer substrate according to claim 24, wherein said metal layer is selected from one of solder, nickel gold alloy and a combination of solder and nickel gold alloy.

26. The multiplayer substrate according to claim 21, further comprising a heat sink disposed a top side of said multiplayer substrate.

27. The multiplayer substrate according to claim 21, wherein said first dielectric layers are selected from one of a thermal plastic resin and a thermal setting resin.

28. The multiplayer substrate according to claim 21, wherein said laminating layers are laminated on both two sides of said core substrate.

29. The multiplayer substrate according to claim 21, wherein said laminating layers are laminated on one side of said core substrate.

30. The multiplayer substrate according to claim 21, further comprising a heat sink disposed a top side of said multiplayer substrate.